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| 09/989,777 | 11/19/2001 | Craig Nemecek | CYPR-CD01208M | 2046 |

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| EXAMINER | |
|---|---|
| SHARON, AYAL I | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/989,777 | NEMECEK, CRAIG |
| | Examiner | Art Unit |
| | Ayal I. Sharon | 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/05,11/28/05*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 1-28 of U.S. Application 09/989,777 filed on 11/19/2001 are currently pending. Claims 21, 25, and 27 have been amended.

### *Specification*

2. The proposed amendment to the specification, filed on 10/12/2005, is objected to because of the following informalities: "09/998,85***6***" should be "09/998,85***9***". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. The prior art used for these rejections is as follows:
5. Profit. Jr., U.S. Patent 5,911,059. (Henceforth referred to as "**Profit**").
6. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

7. **Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Profit.**

8. In regards to Claim 1,

> 1. For a system that includes a device under test and that includes an emulator device:
>
> a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> b) performing a sleep operation, comprising:
>
> > b1) upon receiving a first signal that indicates that a sleep function is to be performed, initiating said sleep function at said device under test;
> >
> > b2) turning off one or more clock of said device under test; and
> >
> > b3) discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

9. In regards to Claim 2,

> 2. The method of Claim 1 wherein said clock comprises an internal CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

10. In regards to Claim 3,

> 3. The method of Claim 2 wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

11. In regards to Claim 4,

> 4. The method of Claim 1 further comprising:
>
> when said sleep function has been completed by said device under test, turning on said clock and sending a second signal from said device under test to said emulator device;
>
> receiving said second signal at said emulator device;
>
> determining the number of clock signals received at said emulator device since said second signal was received; and
>
> resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

12. In regards to Claim 5,

> 5. The method of Claim 4 wherein said device under test further comprises a microcontroller and wherein said first signal comprises a first bit, said first bit received at a register of said microcontroller to indicate that a sleep function is to be performed.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

13. In regards to Claim 6,

> 6. The method of Claim 5 wherein said emulator device further comprises a Field Programmable Gate Array (FPGA) device.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

14. In regards to Claim 7,

> 7. For a system that includes a device under test and that includes an emulator device:
>
> a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> b) performing a stall operation, comprising:
>
> > b1) said device under test conveying clock signals to said emulator device;
> >
> > b2) upon receiving a first signal that indicates that a stall function is to be performed, initiating said stall function at said device under test;
> >
> > b3) upon receiving said first signal, discontinuing said sending of said clock signals from said device under test to said emulator device; and
> >
> > b4) discontinuing execution of said instructions that are performed in lock-step at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

15. In regards to Claim 8,

> 8. The method according to claim 7 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA), said clock signals further comprising signals from said microcontroller central processing unit clock.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

16. In regards to Claim 9,

> 9. The method of Claim 8 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said instructions that are performed in lock-step.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

17. In regards to Claim 10,

> 10. A method for performing a sleep operation, comprising:
>
> executing a sequence of instructions by a device under test, said device under test including at least one clock for generating clock signals;
>
> executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> receiving a first signal at a register of said device under test that indicates that a sleep function is to be initiated;
>
> initiating said sleep function at said device under test upon receipt of said first signal;
>
> turning off said at least one clock of said device under test; and
>
> discontinuing execution of instructions that are performed in lock-step by
>
> said emulator device upon said turning off of said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

18. In regards to Claim 11,

> 11. The method according to claim 10 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

19. In regards to Claim 12,

> 12. The method of Claim 11 wherein said at least one clock includes a microcontroller CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

20. In regards to Claim 13,

> 13. The method of Claim 12 further comprising:
>
> when said sleep function has been completed by said device under test, resuming generation of clock signals at said device under test and coupling said clock signals to said emulator device;
>
> when said sleep function has been completed by said device under test, sending a second signal from said device under test to said emulator device;
>
> receiving said second signal at said emulator device;
>
> determining the number of clock signals received at said emulator device since said second signal was received; and
>
> resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

21. In regards to Claim 14,

> 14. The method according to claim 13 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

22. In regards to Claim 15,

> 15. The method of Claim 14 wherein said first signal is a first bit, said sleep function initiated upon the receipt of said first bit at a register of said microcontroller.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

23. In regards to Claim 16,

> 16. A method for performing a stall operation, comprising:
>
> executing a sequence of instructions by a device under test;
>
> executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> said device under test sending clock signals to said emulator device; receiving a first signal at a register of said device under test that indicates that a stall function is to be initiated;
>
> initiating said stall function at said device under test upon receipt of said first signal;
>
> discontinuing said sending of said clock signals from said device under test to said emulator device upon initiation of a stall function at said device under test; and
>
> discontinuing execution of said sequence of instructions at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

24. In regards to Claim 17,

> 17. The method according to claim 16 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

25. In regards to Claim 18,

> 18. The method according to Claim 17 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

26. In regards to Claim 19,

> 19. The method of Claim 18 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

27. In regards to Claim 20,

> 20. The method of Claim 19 wherein said sequence of instructions comprises the core processing functions of said microcontroller.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Examiner finds that the RUN/HALT of the target program applies to all processing functions of the target program 22.

28. In regards to Claim 21,

> 21. An in-circuit emulation system comprising:
>
> a device under test that executes a sequence of instructions, said device under test operable, upon receiving a first signal, to initiate a stall function;
>
> an emulator device for emulating the functions of said device under test, said emulator device operable so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device configured for receiving clock signals sent by said device under test; and
>
> wherein said device under test sends clock signals to said emulator device, said device under test operable, upon receiving said first signal, to discontinue sending said clock signals to said emulator device, and said emulator device operable, upon said discontinuation of said clock signals from said device under test, to discontinue execution of said sequence of instructions.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

29. In regards to Claim 22,

> 22. The in-circuit emulation system of Claim 21 wherein said device under test is a microcontroller, said microcontroller operable to resume sending said clock signals to said emulator device when said stall function has been completed by said microcontroller, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

30. In regards to Claim 23,

> 23. The in-circuit emulation system of Claim 22 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

31. In regards to Claim 24,

> 24. The in-circuit emulation system of Claim 23 wherein said emulator device comprises a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

32. In regards to Claim 25,

25. An in-circuit emulation system comprising;

a device under test that executes a sequence of instructions, said device under test operable, upon receiving a first signal, to initiate a sleep function at said device under test and to turn off a clock of said device under test; and

an emulator device for emulating the functions of said device under test, said emulator device operable so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device operable, upon said turning off of said clock to discontinue execution of said sequence of instructions at said emulator device.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

33. In regards to Claim 26,

26. The in-circuit emulation system of Claim 25 wherein said device under test comprises a microcontroller, said device under test operable when said sleep function has been completed by said device under test to turn on said at least one clock and to send a second signal to said emulator device, said emulator device operable upon receiving said second signal to determine the number of clock signals received at said emulator device since said second signal was received and said emulator device operable to resume execution of said sequence of instructions when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

34. In regards to Claim 27,

> 27. The in-circuit emulation system of Claim 26 wherein 22 device under test is a microcontroller, said at least one clock further comprising a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

35. In regards to Claim 28,

> 28. The in-circuit emulation system of Claim 27 wherein said emulator device comprises a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

## ***Response to Amendment***

### Re: Oath / Declaration

36. Applicant's amendment to the specification filed on 10/12/2005, and IDS filed on 11/28/05, remedy the objections to the declaration that were presented in the previous Office Action. Those objections have been withdrawn.

*Re: Drawings*

37. Applicant's new drawings filed 10/12/2005 overcome the previous objections to the drawings. The objections to the drawings have been withdrawn.

*Re: Specification*

38. Applicant's proposed amendment to the specification has been objected to due to a minor informality (a typographical error).

*Re: Double Patenting*

39. Applicant's terminal disclaimer to U.S. Patent Application 09/975,030, filed on 10/12/2005, has been entered into the record. The provisional double patenting rejection on the basis of the 09/975,030 has been withdrawn.

40. After further review, Examiner is withdrawing the double patenting rejections based on the following co-pending applications (now issued patents). The issued claims are distinct from the pending claims in the instant application.

    a. Claim 1 of co-pending Application No. 09/998,834, now U.S. Patent 6,957,180.

    b. Claim 4 of co-pending Application No. 09/998,859, now U.S. Patent 6,922,821.

41. After further review, Examiner is withdrawing the double patenting rejections based on the following co-pending applications (now issued patents). The co-

pending claims are sufficiently distinct from the pending claims in the instant application.

a. Claim 1 of co-pending Application No. 09/975,105
b. Claim 1 of co-pending Application No. 09/975,338
c. Claim 1 of co-pending Application No. 09/992,076
d. Claim 1 of co-pending Application No. 10/001,477
e. Claim 1 of co-pending Application No. 10/001,478
f. Claim 1 of co-pending Application No. 10/001,568
g. Claim 1 of co-pending Application No. 10/004,039
h. Claim 1 of co-pending Application No. 10/004,197

*Re: Claim Rejections - 35 USC § 112*

42. Applicant's amendments to claims 21 and 25, filed 10/12/2005, overcome the previously applied 35 USC § 112 rejections. These rejections have been withdrawn.

*Re: Claim Rejections - 35 USC § 102*

43. According to MPEP § 2131, "The elements [in the prior art] must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required." *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

44. The Applicant unpersuasively argues (see amendment filed 10/12/2005, p.14) that the Profit reference teaches the emulation of "target *circuitry*", while the instant application refers to an emulation of a "device under test." Examiner finds these two terms to be interchangeable, because the "device under test" is a circuit.

45. The Applicant unpersuasively argues (see amendment filed 10/12/2005, p.15):

> ... the hardware simulator of Profit is principally a processor model shell, which simulates activity at the target processor's pins; it does not emulate the processor's functionality, see col.6, ln:25-48. Applicants assert that Profit does not disclose emulating the functions of a device under test.

Examiner respectfully disagrees with Applicant's interpretation of the Profit reference.

The Applicant refers to "processor model shell" (Fig.7, Item 212) that is inside the "hardware simulator" (Fig.7, Item 210), but ignores the "processor emulator" (Fig.7, Item 202). The "processor emulator" includes a "processor" (Fig.7, Item 204), a "memory" (Fig.7, Item 202), and a "target program" (Fig.7, Item 22), as well as an interface between the processor and the memory (Fig.7, Item 208).

Profit expressly teaches the relationship between the "hardware simulator" and the "processor emulator" as follows (see Profit, col.5, line 49 to col.6, line 5. Emphasis added):

> The present invention allows for the early simulation of the target hardware and permits the **parallel development of the target hardware and the target program**. The system of the present invention also allows the extensive use of existing debugging tools to aid the developer in the development and integration of the target system. The system combines

> interacting elements of hardware and executing software, **in part by physical emulation and in part by abstract software simulation.**
>
> A preferred embodiment of a testing system 200 according to the present invention is shown in FIG. 7. The system 200 includes three principal components, a processor emulator 202, a communications interface 220, and a host computer 214. In the system 200, **part of the target hardware is modeled by the processor emulator 202 and part of the target hardware is modeled by a hardware simulator 210 running on the host computer 214.** Specifically, the processor emulator 202 models the target processor, and the hardware simulator 210 models the target circuitry. The communications interface 220 facilitates communication between the processor emulator 202 and the hardware simulator 210.

In light of the cited teachings in the Profit Reference, Examiner disagrees with Applicant's assertion that "Profit does not disclose emulating the functions of a device under test."

46. The Applicant unpersuasively argues (see amendment filed 10/12/2005, p.15):

> The rejection also suggests that Profit discloses operating in lock-step fashion with the device under test, as claimed. However, the portion of Profit offered to show this element do [sic] not show lock step operation. Profit describes the operation of the simulation time keeper circuit, which may serve as a clock to keep the processor emulator and the hardware emulator running synchronously; see col. 10, ln. 32 through col.11, ln 43. However, as noted previously, the hardware simulator emulates the operation of the target circuitry; it does not emulate the device under test, as claimed.

Examiner respectfully disagrees with Applicant's argument that "the hardware simulator ... does not emulate the device under test, as claimed". Examiner finds the terms "target circuitry" and "device under test" to be interchangeable, because the "device under test" is a circuit.

In regards to "lock step" operation, Examiner refers the Applicant to the following teaching in Profit (see col.7, lines 55-63. Emphasis added.):

> The communications interface 220 includes a controller 228 which may be implemented with a conventional microprocessor. The controller 228 is coupled to a memory 230 which stores a control program executed by the controller. The controller 228 is the component of the communications interface 220 which manages communications between the process emulator 202 and the hardware simulator 210 and controls the **synchronization** of the target program 22 and the operation of the simulated target circuit.

47. Finally, the Applicant unpersuasively argues (see amendment filed 10/12/2005, p.15. Emphasis added):

> Moreover, Profit's example of the interaction between the target microcontroller and the hardware simulator **does not suggest running the microcontroller code on both**. Instead, the hardware simulator receives instructions from the microcontroller to execute certain behaviors, and converts interrupts and other events into processor functions that allow the target program executing in the processor emulator to handle the interrupt or event; see col. 6, ln. 25-47.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "running the microcontroller code on both [the target microcontroller and the hardware simulator]") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Moreover, Examiner respectfully disagrees with Applicant's interpretation of the Profit reference. Profit expressly teaches the relationship between the "hardware simulator" and the "processor emulator" as follows (see Profit, col.7, lines 31-47. Emphasis added):

> The communications interface 220 performs two primary functions. First, it controls communication between the processor emulator 202 executing the target program 22 and the hardware simulator 210 executing the software simulation of the target circuit. Such communication occurs when the communications interface 220 determines that an event in the target program 22 requires access to the target circuit, or when an event in the target circuit needs access to the target program 22. An event in the target program 22 requiring interaction with the target circuit may be, for example, a reference (read or write) to an area of memory allocated to the target circuit, a reference to an I/O device simulated by the target circuit, or an instruction dealing with explicit hardware functions, such as RESET. Conversely, an event in the target circuit requiring interaction with the target program 22 may be, for example, an interrupt request generated by a target circuit component modeled in the hardware simulator 210.

Examiner finds that this interaction corresponds to Applicant's argument of "running the microcontroller code on both [the target microcontroller and the hardware simulator]".

### *Conclusion*

48. Applicant's arguments filed 10/12/2005 have been fully considered but they are not persuasive.

49. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### *Correspondence Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
December 14, 2005

Paul L. Rodriguez 12/15/05
Primary Examiner
Art Unit 2125